WHAT IS CLAIMED IS:

1. A magnetic memory device comprising:

first wirings which run in a first direction and are divided in a second direction different from the first direction;

a second wiring which runs in the second direction; and

a first magneto-resistive element which is arranged across the first divided wirings near an intersection of the first and second wirings in a first memory cell region.

2. A device according to claim 1, wherein the first wirings are divided on the same plane.

3. A device according to claim 1, wherein a distance between the first wirings is shorter than a length of the first magneto-resistive element in the second direction.

4. A device according to claim 1, wherein an intensity of a magnetic field generated upon supplying a current to the first wirings has a plurality of maximum values within a plane of the first magneto-resistive element.

5. A device according to claim 4, wherein the maximum value exists at an end of the first magneto-resistive element.

6. A device according to claim 1, wherein the second wiring is divided into a plurality of wirings in

the first direction.

7. A device according to claim 6, wherein a distance between the second divided wirings is shorter than a length of the first magneto-resistive element in the first direction.

8. A device according to claim 1, wherein the first wirings include word lines.

9. A device according to claim 1, wherein the first wirings include bit lines.

10. A device according to claim 1, wherein, of the first divided wirings, one wiring is arranged in contact with the first magneto-resistive element, and the other wiring is arranged apart from the first magneto-resistive element.

11. A device according to claim 10, wherein

said one wiring is used as a write/read wiring for the first magneto-resistive element, and

said other wiring is used as a write wiring for the first magneto-resistive element.

12. A device according to claim 10, wherein the first magneto-resistive element has a first step.

13. A device according to claim 10, which further comprises

a second memory cell region adjacent to one side of the first memory cell region,

a third memory cell region adjacent to the other side of the first memory cell region,

a second magneto-resistive element which is arranged in the second memory cell region, and

a third magneto-resistive element which is arranged in the third memory cell region, and

in which said one wiring runs from the first memory cell region into the second memory cell region, and is arranged apart from the second magneto-resistive element, and

said other wiring runs from the first memory cell region into the third memory cell region, and is arranged in contact with the third magneto-resistive element.

14. A device according to claim 13, wherein

said one wiring is used as a write wiring for the second magneto-resistive element, and

said other wiring is used as a write/read wiring for the third magneto-resistive element.

15. A device according to claim 13, wherein

the second magneto-resistive element has a second step, and

the third magneto-resistive element has a third step.

16. A device according to claim 1, wherein the first divided wirings are connected in a peripheral circuit region outside the first memory cell region.

17. A device according to claim 16, wherein a wiring pitch between the first wirings is different

between the first memory cell region and the peripheral circuit region.

18. A device according to claim 1, which further comprises

a fourth memory cell region adjacent to the first memory cell region in the first direction, and

a fourth magneto-resistive element which is arranged in the fourth memory cell region, and

in which one of the first divided wirings is used as a write wiring of the fourth magneto-resistive element.

19. A device according to claim 1, wherein a width of each the first wirings is shorter than a length of the first magneto-resistive element in the second direction.